UNIVERSITY OF ENGINEERING AND MANAGEMENT,JAIPUR

Lecture-wise Plan

Subject Name: Processor Architecture for VLSI **Subject Code-MVLSI 201**
Year: 1ST Year **Semester: 2ND**

Module Number	Topics	Number of Lectures
1	**CPU design**	**6L**
	Basic organization of the stored program computer and operation sequence for execution of a program.	2L
	Fetch, decode and execute cycle, Concept of operator, operand, registers and storage, Instruction format. Instruction sets and addressing modes.	4L
2	**CPU design - Timing and control**	**2L**
	Timing diagram and control design	2L
3	**Micro programmed control**	**3L**
	Concepts of Micro operations	3L
4	**Pipeline concept**	**5L**
	Instruction and Arithmetic Pipelining,	2L
	data hazards, control hazards and structural hazards, techniques for handling hazards.	1L
	Pipeline optimization techniques	2L
5	**ALU Design**	**7L**
	Restoring Division Algorithm, Non- Restoring division,	3L
	Multiplier, Different adders.	4L
6	**Superscalar arch:**	**3L**
	Parallel computation	1L
	Ways of parallelism, the IBM PowerPC	2L
7	**VLIW arch**	**3L**
	TI TMS320C6x, advancement to **EPIC**	3L
8	**Coprocessor Approach**	**4L**
	Need for accelerators, Accelerators and different types of parallelism,	2L
	Processor architectures and different approaches to acceleration	2L
9	**Processors using course-grain parallelism:**	**3L**
	utilization of course-grain parallelism**,** chip-multiprocessors**,** multithreaded processors, SMT proc	3L

Faculty In-Charge HOD, ECE Dept.

Assignments

Module 1

1. What do you mean by instruction format? What are the information instruction would convey to the CPU? What are the basic instruction types? Explain how we can reduce the instruction size.

Module 4

1. What do you mean by Instruction Pipeline? Discuss the hardware requirement for implementation of pipeline.

Module 5

1. What the steps to perform restoring division? Draw the block diagram
2. Write short note.
   (a) Sequential Multiplier.
   (b) Carry Look Ahead Adder.
   (c) Non- restoring Divider

UNIVERSITY OF ENGINEERING AND MANAGEMENT,JAIPUR

Lecture-wise Plan

Subject Name: Digital Signal Processing and Applications **Subject Code-MVLSI202**
Year: 1st Year **Semester: Second**

Module Number	Topics	Number of Lectures
1	**Discrete time signal and system in time domain: -**	**8L**
	1. Introduction of DSP and its applications.	1
	2. Type of digital signals, sampling theorem, Shannon's theorem and aliasing effect	1
	3. Various operation of digital signals.	1
	4. Discrete time system	2
	5. Concept of various type of convolution and its properties	2
	6. Concept of correlation and its application	1
2	**Harmonics Analysis of Signals**	**8L**
	1. Brief introduction of Fourier transform	1
	2. Discrete Time Fourier Transform and its properties	1
	3. Some numerical on DTFT	1
	4. Discrete Fourier Transform and its properties	1
	5. Some numerical on DFT	1
	6. Concept of Overlap save and overlap add method	1
	7. Concept of FFT and its application	1
	8. 2 Radix FFT algorithms	1
3.	**Z Transform:**	**5L**
	1. Brief introduction of Z transform and ROC with properties	1
	2. Z transform and its properties	1
	3. Some numerical on Z transform	1
	4. Analysis and designing the system using z transform	2
4	**LTI DTS in frequency domain: -**	**3L**
	1. Introduction of Transfer function and frequency response	1
	2. Introduction of linear phase filter, Group d and phase delay.	1
	3. Concept of simple analog and digital filter	1
5	**Digital FIR Filter design:-**	**6L**
	1. Introduction of FIR filter and its structure	1
	2. Discrete parallel and cascade FIR filter	1
	3. Introduction of Linear phase filter and its characteristics	1
	4. Basic concept of window signal and window functions	1

	5. FIR filter design using various window function	1
	6. design high pass, low pass and band pass filter designing	1
6	**Digital IIR Filter design: -**	**4L**
	1. Introduction of IIR filter and its structure	1
	2. Discrete parallel and cascade IIR filter	1
	3. Basic concept of bilinear transform	1
	4. IIR filter design using bilinear transform	1
7	**DSP processor (TMS 320C 54X):**	**4L**
	1. Introduction of DSP processor and its applications	1
	2. Characteristic and features of TMS 320 DSP family	1
	3. Functional block diagram and architecture of TMS 320C 54X series DSP processor	1
	4. Addressing mode and instruction set of TMS 320C 54X	1

Faculty In-Charge HOD, ECE

Assignment:

Module-1 (Discrete time signal and system in time domain):

1. (a) If x(n) = 0 for n < 0, derive an expression for x(n) in terms of its even part, $x_e(n)$, and, using this expression, find x(n) when $x_e(n) = (0.9)^{|n|}u(n)$.

   (b) If $x_1(n)$ is even and $x_2(n)$ is odd, what is $y(n) = x_1(n) \cdot x_2(n)$?

2. Determine whether or not the signals below are periodic and, for each signal that is periodic, determine the fundamental period.

   (a) $x[n] = \text{Re}\{e^{jn\pi/12}\} + \text{Im}\{e^{jn\pi/18}\}$
   (b) $x[n] = e^{jn\pi/16}\cos(n\pi/17)$

3. Given the sequence x(n) = (6 - n)[u(n) - u(n - 6)], make a sketch of
   (a) $y_1(n)=x(4-n)$
   (b) $y_1n) = x(n^2 - 2n + 1)$

4. Consider the sequence

   $x(n) = \left(\frac{3}{2}\right)^n u(-n)$

(a) Find out the Energy of x(n)
(b) Find out the Power of $x^2(n)$

5. Determine which systems are Liner, shift invariant and causal
   (a) y(n) = x(n)sin(nπ/2)
   (b) y(n) = Re{x(n)}

6. (a) Find the convolution of the two finite-length sequences:
   x(n) = 0.5n[u(n) - u(n-6)] and h(n) = 2sin(nπ/2)[u(n+3) – u(n-4)]
   (b) If the response of a linear shift-invariant system to a unit step (i.e., the step response) is

   $s(n) = n(1/2)^n u(n)$. Find the unit sample response, h(n).

7. Find the periodic convolution of the two finite-length sequences:
   x[n] = [1,4,**-3**,6,4] and h[n] = [2,**-4**,3]……[by using circular matrix method]

8. Two causal finite length sequences are given following.
   y[n] = [6,11,-13,16,1,9,2] and h[n] = [2,5,-1,4]
   If y[n] = h[n]*x[n], then find out the sequence x[n].

Module-2 (Harmonics Analysis of Signals):

1. The DFT of a discrete sequence x[n] is X[k] = [1,2,3,4]
(a) Find out the DFT of the sequence g[n] = x[n-2].
(b) Find out the IDFT of sequence of X[k] = [3, 4, 1, 2].
(c) Find out the value of 'a' and 'b' from the given DFT of x[n] is
X[k] = [0, a, 2+j, -1, b, j].

2. If x[n] = [1,-2,3,-1,5,-9], find out the value of
(a) X[0],
(b) X[3],
(c) $\sum_{k=0}^{5} X[k]$,
(d) $\sum_{k=0}^{5}(-1)^k X[k]$
(e) $X[9]$

3. (a) What is the difference between DTFT and DFT.
(b) Explain how the DFT is coming from DTFT.
(c) What is Twiddle factor?

4. Find out the DFT of given sequence by using matrix method
x[n] = del{n] + 2del[n-1] + del[n-2] +2del[n-3]

5. Determine the Fourier transform of the signal:$x(n) = 2^n u(n) – 2^{-n} u(-n)$.

6. Determine sectional convolution whose impulse response is h[n] = {1,1,1} and input is x[n] = {3, –1,0,1,3,2,0,1,2,1} using overlap add method.

Module-3(Z Transform):

1. If the z transform of x[n] is $32/(Z^2-16)$, then calculate the z transform of $(1/2^n)$ x[n]

2. The transfer function of a causal system is given as
   $H(Z) = (Z+0.5)\,(Z+2)\,(Z-1)^2/Z^4$,
   then calculate the inverse z transform of H(Z).

3. The transfer function of a causal system is given as $H[Z] = \frac{5Z^2}{Z^2-Z-6}$,
   then calculate the value of h[n].

4. Describe correlation and multiplication property of z-transform.

5. Find the inverse Z transform of $X(Z) = \frac{Z(Z^2-4Z+5)}{(Z-3)(Z-1)(Z-2)}$
   for ROC- i) $2 < |Z| < 3$
   ii) $|Z| > 3$
   iii) $|Z| < 1$

6. Find out the Z transform of following signal
   $x[n] = (-1)^n \cos(\pi/3n)\, u[n]$

7. Write down the difference equation for Transfer function

$$H(Z) = \frac{1 + \left(\frac{1}{4}\right)Z^{-1} + \left(\frac{1}{2}\right)Z^{-2} + \left(\frac{1}{3}\right)Z^{-3}}{1 + Z^{-1} + \left(\frac{1}{4}\right)Z^{-2} - \left(\frac{1}{3}\right)Z^{-3} + \left(\frac{1}{2}\right)Z^{-4}}$$

Module-4 (LTI DTS in frequency domain):

1. (a) Find out the impulse response of given system equation
   $y[n] = x[n] + 2x[n-1] - 4x[n-2]$
   (b) Calculate and draw the frequency and phase response of above system.
   (c) How do you explain the nature and properties of the above system?

2. Prove that the IIR filter is always a nonlinear phase filter.
3. Find out the solution of difference equation of
   $y[n] - (1/6)\, y[n-1] - (1/6)\, y[n-2] = 4x[n]$
   if $x[n] = u[n]$, $n \geq 0$, and $y[-1] = 0$, $y[-2] = 12$.

4. The signal $x[n] = \{1, 0.5\}$ is applied to a digital filter and the resulting output is $y[n] = del[n] - 2del[n-1] - del[n-2]$.
   (a) What is the frequency response $H(F)$ of this filter?
   (b) Find the impulse response $h[n]$ of this filter.
   (c) Find the filter difference equation

UNIVERSITY OF ENGINEERING AND MANAGEMENT,JAIPUR

Lecture-wise Plan

Module-5 (Digital FIR Filter design):

1. What type of window(s) may be used to design a low-pass filter with a passband cutoff frequency $\omega_p = 0.35\pi$, and transition width $\Delta\omega = 0.025\pi$, and a maximum stopband deviation of $\delta_s = 0.003$?
2. Use the window design method to design a minimum-order low-pass filter with a passband cutoff frequency $\omega_p = 0.45\pi$, a stopband cutoff frequency $\omega_s = 0.5\pi$, and a maximum stopband deviation $\delta_s = 0.005$.
3. Suppose that we would like todesign a low-pass filteroforder N = 128with a passband cutoff frequency $\omega_p = 0.48\pi$ and a stopband cutoff frequency of $\omega_s = 0.52\pi$
   (a) Find the approximate passband and stopband ripple if we were to use a Kaiser window design.
   (b) If an equiripple filter were designed so that it had a passband ripple equal to that of the Kaiser window designfound in part *(a),* how small would the stopband ripple be?
4. We would like to design an equiripple low-pass filter of order N =30. For a type I filter of order N, what is the minimum number of alternations that this filter may have. and what is the maximum number?
5. For a low-pass filter with $\delta_s = \delta_p$,, what is the difference in the stopband attenuation in decibels between a Kaiserwindow design and an equiripple filter if both filters have the same transition width?

Module-5 (Digital IIR Filter design):

1. Find the minimum order and the 3-dB cutoff frequency of a continuous-time Butterworth filter that will satisfy thefollowing Frequency response constraints:
   $|H(j\Omega)| = 0.95 \qquad \Omega = 16{,}000\pi$
   $|H_a(j\Omega)| \leq 0.1 \qquad \Omega > 24{,}000\pi$
2. Use the bilinear transformation to design a first-order low-pass Butterworth filter that has a 3-dB cutoff frequency$\omega_c = 0.5\pi$.
3. Use the bilinear transformation to design a second-order bandpass Butterworth filter that has 3-dB cutoff frequencies$\omega_l = 0.4\pi$ and $\omega_u = 0.6\pi$.
4. If the specifications for an analog low-pass filter are to have a I-dB cutoff frequency of 1 kHz and a maximum
   stopband ripple $\delta_s = 0.01$ for *If* $|f| > 5$ kHz, determine the required filter order for the following:
   (a) Butterworth filter
   (h) Type **1**Chebyshev filter
   (c) Type I1 Chebyshev filter
   (d) Elliptic filter
5. If an analog filter has an equiripple passband, will the digital filter designed using the impulse invariance method
   have an equiripple passband? Will it have an equiripple passband if the bilinear transformation is used?
6. Can an analogallpass filter be mapped to a digital allpass filter using the bilinear transformation?

7. An IIR low-pass digital filter is to be designed to meet the following specifications:
Passband cutoff frequency of $0.221\pi$with a passband ripple less than ***0.01***
Stopband cutoff frequency of $0.241\pi$with a stopband attenuation greater than ***40*** dB
(a) Determine the filter order required to meet these specifications if a digital Butterworth filter is designed usingthe bilinear transformation.
(b) Repeat for a digital Chebyshev filter.
(c) Compare the number of multiplications required to compute each output value using these filters, and comparethem to an equiripple linear phase filter.

UNIVERSITY OF ENGINEERING AND MANAGEMENT,JAIPUR

Lecture-wise Plan

Subject Name: Analog IC Design **Subject Code-MVLSI 203**
Year: 2ND Year **Semester: 2ND**

Sl. No	*Topic(S)*	
1	***Module – 1:Pre-requisites***	**5L**
	Recompilation of CMOS models for analog circuits - Small signal equivalent circuit	1L
	Recompilation of CMOS models for analog circuits - Temperature effect and sensitivity, overview of electrical noise	1L
	CMOS switch, resistors, current source, sink	1L
	Current mirror, voltage and current references	1L
	MOSFET Model ling for Circuit Simulation	1L
2	***Module – 2: CMOS Amplifiers & CMOS Operational Amplifiers***	**7L**
	Introduction of amplifier, Basic concepts , Performance Parameters	1L
	One state OPAMP, Two stage OPAMP	1L
	Stability and Phase compensation, CASCODE OPAMP	1L
	Design of two- stage amplifier	1L
	Design of CASCODE OPAMP	1L
	High performance CMOS OPAMPs	1L
	Micro-power OPAMP	1L
3	***Module 3: Switch Capacitor circuits***	**4L**
	Introduction, General considerations	1L
	Switched capacitor integrator circuits	1L
	First order switched capacitor filter circuits	1L
	second order switched capacitor filter circuits	1L
4	***Module -4: Data Converter Fundamentals & Architecture***	**6L**
	Introduction, Ideal D/A converters, Ideal A/D converter	1L
	Serial and Flash D/A converters	1L
	Serial and Flash A/D converters	1L
	Medium and High Speed converters	1L
	Over- sampling converters	1L
	converter performance limitations, Design consideration	1L
5	***Module -5: Special CMOS Analog Circuits***	**4L**
	Introduction and CMOS voltage controlled oscillators	1L
	Ring oscillators	1L
	Phase locked loops with pump phase comparators	1L
	G_m-C Circuits	1L
6	***Module -6:*****RF Analog Circuits & Sub-circuits**	**6L**
	Introduction, Capacitors and Inductors in VLSI circuits	1L
	Bandwidth estimation techniques	1L
	Design of high frequency amplifiers	1L
	Design of low noise amplifiers	1L
	Design of Mixers of RF power amplifiers	1L
	Architectures of RF receivers and transmitters	1L

7	***Module -7:CMOS* Comparators**	**5L**
	Introduction and comparator Characterization	1L
	Two state open loop comparators	1L
	Discrete time comparators	1L
	High speed comparator circuits	1L
	CMOS S/H circuits	1L

Faculty In-Charge HOD, ECE Dept.

UNIVERSITY OF ENGINEERING AND MANAGEMENT,JAIPUR

Lecture-wise Plan

Subject Name: Quantum and Nano Science **Subject Code-MVLSI 204**
Year: 2ND Year **Semester: 2ND**

Module No.	*Topic(S)*	Number of Lectures
1	***Module – 1:* Quantum & Statistical Mechanics**	**9L**
	Wave particle duality and Schrodinger equation	1L
	Free and bound particles	1L
	Eigen functions	1L
	Quantum mechanical operators	1L
	Probability current density	1L
	Particle in square well potential	1L
	Maxwell-Boltzmann statistics	1L
	Bose-Einstein and Fermi-Dirac statistics	1L
	Concept of phonons	1L
2	***Module – 2:* Quasi Low-Dimensional Structures**	**6L**
	Quantum wells, Wires, Dots	1L
	Band structure of low-dimensional systems	1L
	Quantum confinement	1L
	Density-of states in 2D, 1D and 0D structures	1L
	Heterostructures and bandgap engineering	1L
	Modulation doping, Strained layer structures	1L
3	***Module 3:* Electrical and Optical Properties of Low-Dimensional Systems**	**9L**
	Infinitely deep square wells	1L
	Wells of finite depth	1L
	Parabolic wells	1L
	Superlattices; Scattering mechanisms	1L
	Mobility enhancement	1L
	Tunneling in heterostructures	1L
	Quantum Hall effect	1L
	Optical absorption in quantum wells: Intersubband transitions	1L
	Quantum well laser, Resonant tunneling	1L
4	***Module -4:* Physics of Nanostructure Devices**	**3L**
	Single electron transistors: Coulomb block phenomenon	1L
	Fabrication and applications, Memory devices	1L
	Quantum computer, Spintronics, Molecular electronic devices	1L
5	***Module -5:* Carbon Nanotubes**	**3L**
	Types of nanotubes and their formation	1L
	Properties of nanotubes, Uses in nanoelectronics	1L
	Carbon nanotube transistors, Future prospect.	1L

Faculty In-Charge HOD, ECE Dept.

UNIVERSITY OF ENGINEERING AND MANAGEMENT,JAIPUR

Lecture-wise Plan

Subject Name: Mobile Communication **Subject Code-MVLSI 205**
Year: 2ND Year **Semester: 2ND**

Module Number	Topics	Number of Lectures
1	**Introduction**	**3L**
	evolution of mobile radio communications, mobile radio systems around the world,	1L
	trends in cellular radio and personal communication,	1L
	First generation (1G), second generation (2G), third generation (3G) mobile cellular networks.	1L
2	**Cellular concept**	**6L**
	Limitations of conventional mobile system, Introduction to mobile cellular communication,	1L
	Concept of frequency reuse, cluster size, cellular system architecture, channel assignment strategies,	2L
	call handoff strategies - hard handoff and soft handoff, prioritizing handoff; interference and system capacity,	2L
	improving capacity in cellular systems – cell splitting, sectoring, microcell zone concept.	1L
3	**Different mobile communication systems**	5L
	GSM services and features, system architecture, GSM radio subsystem,	1L
	GSM channel types, location updating and call setup, WAP, SCSD, GPRS, EDGE, 3G W-CDMA;	2L
	CDMA digital cellular standard, comparison between GSM and CDMA, 3G cdma2000, IMT-2000.	2L
4	**Radio Channel Characterization**	**4L**
	Free space propagation, Multipath propagation,	1L
	diversity techniques, Co-channel interference, Propagation effects - scattering,	2L
	ground reflection, fading, Log-normal shadowing.	1L
5	**Wireless networks**	3L
	Advantages and applications of Wireless LAN, WLAN technology – RF and IR wireless LAN, diffuse,	1L
	quasi-diffuse and point-topoint IR wireless LAN, IEEE802.11, IEEE802.11 architecture, Physical layer,	1L
	MAC layer, Introduction to WI-FI, HIPERLAN2, Bluetooth – Bluetooth architecture	1L
6	**Mobile network and transport layer**	**6L**
	Introduction to Mobile IP, requirements, IP packet delivery, Agent discovery, Registration	1L
	Tunneling and encapsulation, Optimization, Reverse tunneling;	1L
	Mobile adhoc networks – Routing, Destination sequence distance vector, Dynamic source routing and Alternative metrics; Traditional TCP – Congestion control, Slow start, Fast retransmit / fast recovery, Implications of mobility;	2L

	classical TCP improvements – Indirect TCP, Snooping TCP, Mobile TCP, Fast retransmit. --10L Future of mobile communication – 3G to 4G	2L

Faculty In-Charge HOD, ECE Dept.

UNIVERSITY OF ENGINEERING AND MANAGEMENT,JAIPUR
Lab Manual

Title of Course: Embedded system Lab-II
Course Code: MVLSI-291
L-T-P scheme: 0-0-3 **Course Credit: 3**

Objectives:

An embedded system is some combination of computer hardware and software, either fixed in capability or programmable, that is specifically designed for a kind of application device. Industrial machines, automobiles, medical equipment, cameras, household appliances, airplanes, vending machines, and toys (as well as the more obvious cellular phone and PDA) are among the myriad possible hosts of an embedded system. Embedded systems that are programmable are provided with a programming interface, and embedded systems programming is a specialized occupation. Since the embedded system is dedicated to specific tasks, design engineers can optimize it, reducing the size and cost of the product, or increasing the reliability and performance. Some embedded systems are mass-produced, benefiting from economies of scale.

Learning Outcomes: The students will have a detailed knowledge of the concepts ofembedded system and ARM processor. During this class students, can write a simple and complex assembly language programming using ARM controller. Upon the completion of this practical course, the student will be able to:

- **Understand** the ARM processor.
- **Using**this new processor, they can interface with another co-processor**.**
- **Study**the benefits to use ARM processor in our real life.
- **Analyze** and simulate the various program.
- **Interface**various hardware interface with ARM processor.
- **Implement and simulate** the application based program in proteus environment.

Course Contents:
Exercises that must be done in this course are listed below:

Exercise No.1: Write an assembly language program to add two 64 bit numbers by ARM processor,
Exercise No. 2: Write an assembly language program for addition two 32 bit numbers,
Exercise No. 3: Write an assembly language program to find smallest of N numbers
Exercise No. 4: Write an assembly language program to find largest of N numbers
Exercise No. 5: Write an assembly language program to convert Hex to ASCII
Exercise No. 6: Write an assembly language program to convert ASCII to hex
Exercise No. 7: Write an assembly language program to generate N Fibonacci numbers
Exercise No. 8: Write an ALPto find the factorial of a given number using subroutine
Exercise No. 9: Write an assembly language program to find the multiplication of two 32-bit number

Text Book:

1. William Hohl,"ARM Assembly Language: Fundamentals and Techniques", Second Edition, CRC Press
2. Vincent Mahout, "Assembly Language Programming: ARM Cortex-M3", Wiley publication

Recommended Systems/Software Requirements:

Minimum system requirement: -

Processor	:	AMD Athlon ™ 1.67 GH_z
RAM	:	256 MB
Hard Disk	:	40 GB
Mouse	:	Optical Mouse

Software requirement: - Windows 2007/8/10, keil simulator, ect.

Experiment No: 1

AIM: Write an assembly language program to add two 64 bit numbers by ARM processor

APPARATUS: Computer, Keil software.

PROGRAM:

```
AREA ADDTIN, CODE
ENTRY
ldr r0,=value1
ldr r1,[r0]
ldr r2,[r0,#4]
ldr r0,=value2
ldr r3,[r0]
ldr r4,[r0,#4]
adds r6,r2,r4
adc r5,r1,r3
ldr r0,=result
str r5,[r0]
str r6,[r0,#4]
swi&11
value1 dcd &BBBBBBBB,&AAAAAAAA
value2 dcd &CCCCCCCC,&FFFFFFFF
result dcd &0
```

RESULT: Addition of 64-bit data has been performed successfully by using the software.

UNIVERSITY OF ENGINEERING AND MANAGEMENT,JAIPUR
Lab Manual

Experiment No: 2

AIM: - Write an assembly language program to add two 32 bit numbers by ARM processor

APPARATUS: Computer, Keil software.

PROGRAM: -

```
AREA ADDTIN, CODE
ENTRY
ldr r0,=value1
ldr r1,[r0]
ldr r0,=value2
ldr r2,[r0]
adds r3,r2,r1
value1 dcd &BBBBBBBB
value2 dcd &CCCCCCCC
end
```

RESULT: Addition of 32-bit data has been performed successfully by using the software.

Experiment No: 3

AIM: - Write an assembly language program to find smallest from N numberby ARM processor

APPARATUS: Computer, Keil software.

PROGRAM: -

```
AREA arr,code
        ENTRY
main
        ldr r0,=data1
        ldr r3,=0x40000000
        ldr r4,=0x05    ;//length of loop
        ldr r1,[r0],#04
        sub r4,r4,#01
back
        ldr r2,[r0]
        cmp r1,r2
        bls less              ;// branch on low
        mov r1,r2
less
        add r0,r0,#04
        sub r4,r4,#01
        cmp r4,#00
        bne back
        str r1,[r3]           ;// smallest value stored in memory location
stop b stop
        AREA data,code
data1 dcd &64,&05,&96,&10,&65
        END
```

RESULT: The above program has been performed successfully by using the software.

UNIVERSITY OF ENGINEERING AND MANAGEMENT,JAIPUR
Lab Manual

Experiment No: 4

AIM: -Write an assembly language program to find largest from N numberby ARM processor

APPARATUS: Computer, Keil software.

PROGRAM: -

```
AREA arr,code
        ENTRY
main
        ldr r0,=data1
        ldr r3,=0x40000000
        ldr r4,=0x05    ;//length of loop
        ldr r1,[r0],#04
        sub r4,r4,#01
back
        ldr r2,[r0]
        cmp r1,r2
        bhs large                   ;// branch on low
        mov r1,r2
large
        add r0,r0,#04
        sub r4,r4,#01
        cmp r4,#00
        bne back
        str r1,[r3]          ;// smallest value stored in memory location
stop b stop
        AREA data,code
data1 dcd &64,&05,&9,&00,&65
        END
```

UNIVERSITY OF ENGINEERING AND MANAGEMENT,JAIPUR
Lab Manual

Experiment No: 5

AIM: -Write an assembly language program to convert Hex to ASCII by ARM processor

APPARATUS: Computer, Keil software.

PROGRAM: -

```
AREA arr,code
        entry
main
        ldr r0,=value1
        ldr r1,[r0]
        mov r2,r1
        cmp r1,#0x09
        bhigrt
        add r1,r1,#0x30                 ;//add 30 if data <9
        bl nxt1
grt
        add r1,r1,#0x37                 ;//add 37h if data>9
nxt1
        ldr r4,=0x40000000
        str r1,[r4]
stop b stop
        AREA data,code
value1 dcd &07
        END
```

RESULT: The above program has been performed successfully by using the software.

Experiment No: 6

AIM: -Write an assembly language program to convert ASCII to HEXby ARM processor

APPARATUS: Computer, Keil software.

PROGRAM: -

```
AREA arr,code
        entry
main
        ldr r0,=value1
        ldr r1,[r0]
        mov r2,r1
        cmp r1,#0x39
        bhigrt
        sub r1,r1,#0x30                 ;//SUB 30 if data <39
        bl nxt1
grt
        sub r1,r1,#0x37                 ;//SUB 37h if data>39
nxt1
        ldr r4,=0x40000000
        str r1,[r4]
stop b stop
        AREA data,code
value1 dcd &41
        END
```

RESULT: The above program has been performed successfully by using the software.

UNIVERSITY OF ENGINEERING AND MANAGEMENT,JAIPUR
Lab Manual

Experiment No: 7

AIM: -Write an assembly language program to generate N Fibonic numbersby ARM processor

APPARATUS: Computer, Keil software.

PROGRAM: -

```
AREA arr,code
        ENTRY
main
        ldr r0,=value
        ldr r1,[r0]
        ldr r2,=0x40000000      ;/*memory location  fibonic series*/
        ldr r9,=0x02
        ldr r3,=0x00
        mov r6,r2
        str r3,[r2],#04
        add r3,r3,#01
        mov r7,r2
        str r3,[r2],#04
back
        ldr r4,[r6],#04
        ldr r5,[r7],#04
        add     r5,r4,r5
        str r5,[r2],#04
        add r9,r9,#01
        cmp r9,r1
        BNE back
stopb stop
        AREA data,code
value dcd &0a           ;/* here ten fibonic numbers are ganerated*/
        END
```

RESULT: The above program has been performed successfully by using the software.

Experiment No: 8

AIM: -Write an assembly language program to find the factorial of a given number using subroutine by ARM processor

APPARATUS: Computer, Keil software.

PROGRAM: -

```
AREA arr,code
        ENTRY
main
ldr r0,=value
        bl fact                 ;// call subroutine fact
        ldr r1,=0x40000000
        str r5,[r1]
stop b stop
        AREA data,code
value dcd &0a
fact
mov r6,r14
        ldr r2,[r0]
        cmp r2,#00
        beq END1
        mov r3,r2
loop
        sub r2,r2,#01
        cmp r2,#00
        mulne r3,r2,r3
        bne loop
        mov r5,r3
        bl END2
END1
```

```
        ldr r5,=0x01
END2
        mov PC,r6          ;// return to main program.
        END
```

RESULT: The above program has been performed successfully by using the software.

Experiment No: 9

AIM: -Write an assembly language program to find the multiplication of two 32 bit numberby ARM processor

APPARATUS: Computer, Keil software.

PROGRAM: -

```
AREA ADDTIN,CODE
        ENTRY
        ldr r0,value1
        ldr r1,value2
umull r4,r3,r1,r0
value1 dcd &BBBBBBBB
value2 dcd &CCCCCCCC
        end
```

RESULT: The above program has been performed successfully by using the software.

UNIVERSITY OF ENGINEERING AND MANAGEMENT,JAIPUR

Lab Manual

UNIVERSITY OF ENGINEERING AND MANAGEMENT, JAIPUR

Course Description

Title of Course: Grand Viva **Course Code: MVLSI281**
L-T –P Scheme: 0-0-0 **Course Credits: 4**

Aims and Objectives

1. To compare the traditional viva examination (TVE) with OSVE (Objective Structured Viva Examination).

2. To obtain the students' opinion regarding OSVE as an assessment tool.

3. A suggestion to include OSVE as a part of university examination.

Materials and Methods

The study was carried out in November 2012, at K.J. Somaiya Medical College, in the department of Anatomy. 50 students were exposed to different stations of viva as well as OSVE. A comparison was made of the student's performance and a feedback was taken from the students regarding the same.

As the OSVE was being conducted for the first time, the students were notified in advance regarding the plan for conducting the part ending practical assessment – by both the TVE and OSVE. The OSVE was planned for 20 marks, viva voce of 20 marks.

Purpose and Format of the Viva Voce Examination

Literally, "viva voce" means by or with the living voice - i.e., by word of mouth as opposed to writing. So the viva examination is where you will give a verbal defence of your thesis.

Put simply, you should think of it as a verbal counterpart to your written thesis. Your thesis demonstrates your skill at presenting your research in writing. In the viva examination, you will demonstrate your ability to participate in academic discussion with research colleagues.

Purpose of the Exam

The purpose of the viva examination is to:

- demonstrate that the thesis is your own work
- confirm that you understand what you have written and can defend it verbally
- investigate your awareness of where your original work sits in relation to the wider research field
- establish whether the thesis is of sufficiently high standard to merit the award of the degree for which it is submitted

- allow you to clarify and develop the written thesis in response to the examiners' questions

The Examiners and Exam Chair

You will normally have two examiners:

- an internal examiner who will be a member of academic staff of the University, usually from your School/Department but not one of your supervisors
- an external examiner who will normally be a member of academic staff of another institution or occasionally a professional in another field with expertise in your area of research (candidates who are also members of University staff will normally have two external examiners in place of an internal and an external examiner)

Your supervisor should let you know who your examiners will be as it is important that you ensure you are familiar with their work and any particular approach that they may take when examining your thesis.

In some cases there may also be a Chair person for the examination. A Chair is appointed if the Graduate Dean or either of the examiners feels this is appropriate, for example where the examining team has relatively little experience of examining UK research degrees. The Chair is there to ensure the examination is conducted in line with University regulations and is not there to examine your thesis. If there is a Chair person, it will usually be a senior member of the academic staff of your School/Department.

Normally no one else is present in the exam.

Exam Venue and Arrangements

Your internal examiner is responsible for arranging your viva exam and they will contact you with the relevant details - date, time, venue, etc.

Usually the viva exam will take place in your School/Department, though occasionally another University location may be used. If you are unsure where you need to go, make sure you check this before the day of your exam.

If you returned your Notice of Intention to Submit Your Thesis three months before your submission date, your viva exam should normally take place quite soon after submission. Almost

all viva exams take place within three months of thesis submission and in many cases it is within one month.

Format of the Exam

All viva examinations are different, so it is not possible to describe exactly what will happen - but there are general points which can be made which may be helpful, and you should have the opportunity before your examination to discuss what will happen with your supervisor or to attend the University's pre-viva examination workshop.

The purpose of the viva is to establish that your work is of a sufficiently high standard to merit the award of the degree for which it is submitted. In order to be awarded a research degree, the thesis should demonstrate an original contribution to knowledge and contain work which is deemed worthy of publication.

In order to do this, examiners may:

- ask you to justify your arguments
- ask you to justify not only things which you have included in your thesis but also things which you may have left out
- ask you questions about the wider research context in which the work has been undertaken
- argue certain points with you
- expect you to discuss any developments which may flow from your work in the future

Inevitably, your thesis will have strengths and weaknesses and the examiners will want to discuss these. It is considered a positive thing, indeed an essential thing, that you can discuss both the strengths and the weaknesses. You can think of the weaknesses as an opportunity to demonstrate your skill at critical appraisal.

Remember that examiners seek to find and discuss weaknesses in all theses - you should not interpret criticism as an indication that the examination will not end successfully.

UNIVERSITY OF ENGINEERING AND MANAGEMENT, JAIPUR

Course Description

Title of Course: Seminar
Course Code: MVLSI282
L-T-P scheme: 0-2-0 **Course Credit: 1**

The overall aim of the seminar series is to help develop an emerging field at the intersection of multi-disciplinary understandings of culture and education. It will build on the existing body of work on education and culture, but its aim is explore and develop new perspectives in this area.
The objectives of the six exploratory seminars are:

- **to explore new research from a range of academic disciplines which sheds light on the questions outlined above**
- **to showcase cutting edge research on education and culture from outstanding academic researchers from the UK and internationally**
- **to bring together seminar participants from different disciplines such as Sociology, Philosophy, Psychology, Human Geography, Media Studies as well as Education and Cultural Studies**
- **to encourage and financially support the participation of PhD students**
- **to actively involve practitioners and users from each venue**
- **to engage a core group of policy makers**
- **to use the seminars to develop links between academics and stakeholders in the arts, library, media, community and educational sectors**